REMARKS

Favorable reconsideration of this application is respectfully requested in view of the amendments above and the following remarks. Claims 1-20 and 23-25 are pending, of which claims 1, 23, and 25 are independent. Claims 21 and 22 were not elected in response to the restriction requirement mailed March 23, 2004 and are canceled herein.

Claims 1-14, 18-20, and 23-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. (6,708,069) in view of admitted prior art. Claims 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. in view of admitted prior art in further view of Kelly (5,734,872). Claims 17 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. in view of admitted prior art in further view of Kardach et al. (5,560,001).

Claims 4 and 6 were objected to as including allowable subject matter but being dependent on a rejected base claim.

Claim 1 was objected to and claims 1-20 were rejected under 35 U.S.C. § 112 second paragraph as being indefinite.

The above rejections and objection are respectfully traversed for at least the reasons set forth below.

Drawing Objection

The drawings were objected to under 37 C.F.R. 1.83(a). The objection states that the programmable logic device and the field programmable gate array (FPGA) in claims 15-16 must be shown or canceled from the claims.

This objection is respectfully traversed. The bus processing block 208 is shown in figures 1 and 2 and may include programmable logic, such as an FPGA. Furthermore, the block 208 shown in figure 2 includes a description of "programmable", which refers to programmable logic, such as an FPGA, as stated in the detailed description. Thus, the Applicant believes that the claimed programmable logic is shown in the figures.

Claim Objection

Claim 1 was objected to because the preamble recited "a circuit arrangement" and "a first circuit arrangement". The Examiner recommended using a first circuit arrangement and a second circuit arrangement to avoid any confusion.

This objection is respectfully traversed. The Applicant's believe that there is no confusion between the terms, because "first" is used to distinguish between the two claimed circuit arrangements. Furthermore, the dependent claims qualify which circuit arrangement is being referenced. For example, claim 5 recites "the first circuit arrangement includes".

Claim Rejection Under 35 U.S.C. §112

Claims 1-20 were rejected claims under 35 U.S.C. § 112 second paragraph as being indefinite. In particular "a programmable device" is recited twice in claim 1. In one instance claim 1 recites "a bus processing block ... with a programmable device", and in a second instance claim 1 recites "a filter circuit ... with a programmable device". Claims 15 and 16 recite "the programmable device" and it was unclear to which programmable device claims 15 and 16 are referencing.

Claim 1 has been amended to recite "a filter circuit ... with a second programmable device". Thus, claims 15 and 16 now reference the programmable device of the bus processing block. No new matter has been added and support for this feature is provided on page 8, line 29-page 9, line 2 of the application.

Claim Rejection Under 35 U.S.C. §103

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

1. Claims 1-14, 18-20, and 23-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. in view of admitted prior art.

Claim 1 recites,

> a bus processing block coupled to the bus interface circuit, the bus processing block implemented with a programmable device and configured to perform selected processing in response to selected bus messages; and
>
> a filter circuit coupled to the bus interface circuit and to the bus processing block, the filter circuit implemented with a second programmable device and configured to direct bus messages to a selected one of the bus interface circuit and the bus processing block.

Ohashi et al. fails to teach or suggest a bus processing block with a programmable device and a filter circuit with a programmable device.

Ohashi et al. discloses a distributed control system including a plurality of nodes, wherein each node includes a processor. See figure 1. Examples of the distributed control system include a semiconductor production system, a home/building automation system, and a medical system.

Ohashi et al. discloses that each of the nodes transmits and receives messages via a transmission line 100. For example, when a node transmits a message, the message is broadcasted on the transmission line 100. Every node connected to the transmission line 100 receives the message and determines whether the message is intended for a respective node by comparing information in the message to information stored in the respective node. A filtering circuit 205 in each node performs the comparison, and thus determines whether a node receiving the message should process the message.

The filtering circuit 205 is shown in detail in figure 3. A message is received and stored in 301. The comparison parts 3031-3033 compare information in the message with information stored in the registration parts 3021-3023. The control part 304 receives the comparison results for each of the comparison parts 3031-3033. If all of the comparison results indicate an "agreement" then the message is stored in 305 and eventually processed by

the CPU 201 of the node. If any of the comparison parts outputs a result of "disagreement", the message is abandoned from the storing part 301. See column 9, lines 34-47.

The rejection of claim 1 states that the bus processing block with a programmable device is taught by the control part 304 shown in figure 3 of Ohashi et al. However, Ohashi et al. fails to teach or suggest the control part 304 is programmable. Ohashi et al. discloses that the control part 304 performs the function of determining whether all the comparison parts 3031-3033 output a result of "agreement" or if any of the comparison parts 3031-3033 output a result of "disagreement". Ohashi et al. does not disclose the function of the control part 304 can be changed. Instead, the control part 304 simply determines whether the comparison results are all in "agreement". This function remains the same regardless of the type of message or the processing to be performed on the message by the CPU. The control part 304 is not programmable and does not include a programmable device.

Similarly, Ohashi et al. fails to teach or suggest that the filter circuit is programmable. The rejection states that the filter circuit is taught by the means to compare the message as disclosed in column 7, last line-column 8, lines 1-4. This section of Ohashi et al. refers to the comparison parts 3031-3033 that compare information in the message with information stored in the node. Each of the comparison parts 3031-3033 outputs an "agreement" or "disagreement" based on the comparison performed by a respective comparison part. Ohashi et al. fails to teach or suggest that the comparison parts 3031-3033 can be programmed or include a programmable device.

In addition, Ohashi et al. fails to teach or suggest a filter circuit configured to direct bus messages to a selected one of the bus interface and the bus processing block. According to an embodiment of the Applicant's invention, the filter circuits 204 or 206 shown in figure

2 select either the bus processing block 208 or the bus interface 202 for processing a message. In one example, messages needing customized processing, which is implemented through the programmable processing block 208 programmed to provide the customized processing, are directed to the processing block 208. Messages not needing the customized processing are directed to the bus interface. Thus, the filters 204 and 206 perform a selection process, which ensures the processing block 208 is not burdened with operations for which customized processing is not desired.

Ohashi et al., on the other hand, fails to teach or suggest selecting either the bus interface or the processing block. Instead, Ohashi et al. discloses that messages outgoing from a node to the transmission line 100 are first transmitted by the node CPU 201 into a storing part 306 in the filter circuit 205 of the node. Messages in the storing part 306 are then transmitted to the transmission line 100. See column 9, lines 49-55. The filter circuit 205 does not perform a selection process and is not configured to direct a message to a selected one of the bus interface and the bus processing block.

Ohashi et al. was combined with the admitted prior art to reject claim 1. However, the admitted prior art also fails to teach or suggest the features described above. Accordingly, claims 1-20 are believed to be allowable.

Independent method claim 23 recites,

> selecting a first class of bus messages for processing by the bus processing block and selecting a second class of bus messages for processing by the bus interface circuit.

Ohashi et al. fails to teach or suggest this feature. The rejection of claim 23 states that the control part 304 of Ohashi et al. performs selected processing in response to selected bus messages.

As described above, a filtering circuit 205 in each node compares information in a received message with stored information to determine whether a node receiving the message should process the message. The control part 304 in the filtering circuit 205 receives the comparison results for each of the comparison parts 3031-3033. If all of the comparison results indicate an "agreement" then the message is stored in 305 and eventually processed by the CPU 201 of the node. If any of the comparison parts outputs a result of "disagreement", the message is abandoned from the storing part 301. Thus, the control part 304 processes all messages by determining whether the messages are in "agreement" or "disagreement". The control part 304, however, does not select a first class of messages for processing by a bus processing block, and does not select a second class of bus messages for processing by a bus interface circuit. In fact, none of the components of the filtering circuit 205 perform the claimed selecting.

Independent claim 25 recites a similar feature, which includes,

> means for selecting a first class of bus messages for processing by the bus processing block and selecting a second class of bus messages for processing by the bus interface circuit.

The claimed selecting recited in claim 23 and the claimed means for selecting recited in claim 25 are not taught or suggested by either Ohashi et al. or the admitted prior art. Thus, claims 23-25 are also believed to be allowable.

2. Claims 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. in view of admitted prior art in further view of Kelly.

Claims 15 and 16 are believed to be allowable for at least the reasons claim 1 is believed to be allowable. In addition, it would not have been obvious to combine the FPGA of Kelly with Ohashi et al. in view of the admitted prior art.

Claims 15 recites the programmable device [of the bus processing block] includes a programmable logic device, and claim 16 recites the programmable device is an FPGA. The rejection substitutes the logic of the processing block of Ohashi et al., which as stated in the rejection is the control part 304, with the FPGAs of Kelly. The stated motivation for this modification and combination is that it would improve performance by employing FPGAs to perform any pre-processing for the CPU. However, simply substituting FPGAs for another type of logic does not improve performance. Thus, the motivation is improper. In addition, there is no need to make the control part 304 of Ohashi et al. programmable. The control part 304 simply determines whether the comparison results are all in agreement. This function remains the same regardless of the type of message or the processing to be performed on the message by the CPU. Thus, there is no need to make the control part 304 programmable. In fact it may be prohibitive to do so, because of increased costs resulting from using FPGAs instead of cheaper logic.

Furthermore, Ohashi et al. and Kelly are unrelated. Kelly is directed to interconnection systems wherein the computer design permits an application-specific choice among several different CPUs. See column 1, lines 9-17. FPGAs are used to provide programmable interconnections between the CPUs and the motherboard to permit application-specific choice among CPUs. See column 3, lines 42-51. Ohashi et al. is

unrelated to the interconnection system of Kelly. Ohashi et al. is directed to handling broadcasted messages in a distributed control system, such as a semiconductor production system, a home/building automation system, and a medical system. Ohashi et al. is not concerned with a programmable interconnection system for a computer system. Thus, it would not have been obvious to one of ordinary skill in the art to combine Kelly with Ohashi et al.

3. Claims 17 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohashi et al. in view of admitted prior art in further view of Kardach et al.

Claims 17 is believed to be allowable for at least the reasons claim 1 is believed to be allowable. In addition, it would not have been obvious to combine the microcode engine of Kardach et al. with Ohashi et al. in view of the admitted prior art.

Claims 17 recites the programmable device [of the bus processing block] includes a microcode engine. The rejection substitutes the logic of the processing block of Ohashi et al., which as stated in the rejection is the control part 304, with the microcode engine of Kardach et al. The stated motivation for this modification and combination is that it would improve performance by employing a microcode engine to perform any pre-processing for the CPU. However, simply substituting a microcode engine for another type of logic does not improve performance. Thus, the motivation is improper. In addition, there is no need to make the control part 304 of Ohashi et al. programmable. The control part 304 simply determines whether the comparison results are all in agreement. This function remains the same regardless of the type of message or the processing to be performed on the message by the CPU. Thus, there is no need to make the control part 304 programmable. In fact in may be

prohibitive to do so, because of increased costs resulting from using programmable logic, such as a microcode engine, instead of cheaper logic.

Furthermore, Ohashi et al. and Kardach et al. are unrelated. Kardach et al. is directed to a method of operating a processor at reduced speed. Ohashi et al. is directed to handling broadcasted messages in a distributed control system, such as a semiconductor production system, a home/building automation system, and a medical system, which is unrelated to controlling processor speed. Thus, it would not have been obvious to one of ordinary skill in the art to combine Kardach et al. with Ohashi et al.

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

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Dated: September 22, 2004 By

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